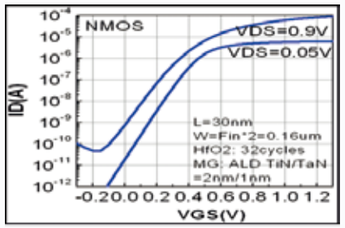
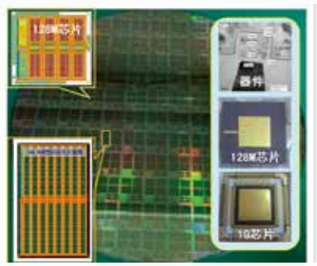
Research Group of the R&D of Key ULSI Technologies, Institute of Microelectronics, Chinese Academy of Sciences



16/14 纳米三维 FinFET 器件特性

Electrical charactertics of 16/14nm 3D FinFETs



1G/128M 大容量高速闪存原型芯片

1Gb/128Mb high speed flash memory prototype chip

The research team, from the Institute of Microelectronics of the Chinese Academy of Sciences (IMECAS), has established and led an Industry-University-Research alliance in ultra-large-scale integration (ULSI) research and development (R&D) nationwide. The alliance is financially supported by the National Sciences & Technologies Major Project. Through tremendous efforts over the past five years, the team, in collaboration with Peking University, Tsinghua University, Fudan University, SMIC, and XMC, has achieved breakthroughs in key ULSI technologies which include 22nm high-κ/metal gate engineering, 14nm FinFET devices, novel flash memory devices, and design for manufacturing. The team has demonstrated world-leading research capabilities in ULSI R&D area.

The team has presented and successfully implemented the Strategy of Intellectual Property-Oriented R&D for ULSI in China. A systematic frame work of IP protection for Chinese ULSI industry, especially in ULSI key process modules, has been established, which consists of 2406 patent applications along with 483 internationals. For the first time, the team has completed IP license to major ULSI manufacturers in China. The transferred technologies are in the development process for massive production.

The achievement of the team has demonstrated that China started to gain a competitive position in the R&D of ULSI, which is highly globalized high-technology. It will provide a strong technical support and boost the upgrading of Chinese ULSI industry for 22nm technology node and beyond.

Outstanding contributors of this research group

Ye Tianchun

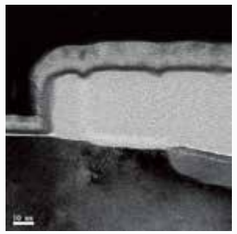
Ye Tianchun is responsible for the overall design and planning of the technology roadmap, and systematic design and implementation of intellectual properties. He is also in charge of the organization of the Industry-University-Research ULSI alliance, as well as the promotion of technology R&D and industrialization.

Chen Dapeng

Chen Dapeng is responsible for the organization of the R&D for 22nm-14nm key process technologies, promotion of the key project tasks, and establishment of the open platform of Integrated Circuit Advanced Process R&D Center.

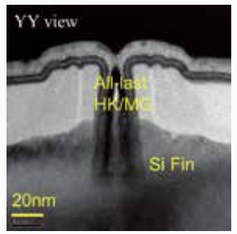
Zhu Huilong

Zhu Huilong is responsible for the key technology development. He has initiated the Strategy of Intellectual Property-Oriented R&D for ULSI in China and has led establishing the 20-14nm key IP portfolios. He was ranked world No. 1 and No. 5, as of 2013, on high-κ/metal gate and FinFET fields, respectively, according to the number of patent applications by individuals.



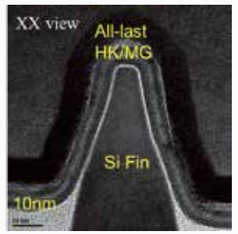
新型硅化物与超浅结

Novel Silicide and Ultra-shallow Junction



16/14 纳米三维 FinFET（YY 截面）

16/14nm 3D FinFET on YY X-view



16/14 纳米三维 FinFET（XX 截面）

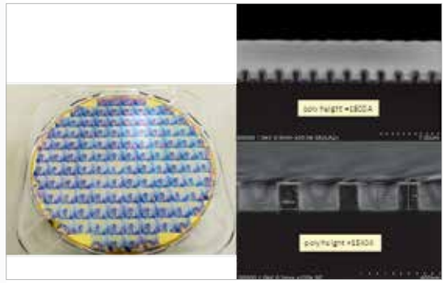
16/14nm 3D FinFET on XX X-view

Other members

Zhao Chao
Min Jiang
Yang Shining
Xu Qiuxia
Liu Ming
Chen Lan
Yin Huaxiang
Zhong Huicai
Yin Haizhou
Li Junfeng
Wang Wenwu
Huo Zongliang
Li Chunlong
Wang Hongli
Wang Dahai
Yuan Wenbiao
Tang Bo

极大规模集成电路关键技术研究集体

研究集体推荐单位：中国科学院微电子研究所

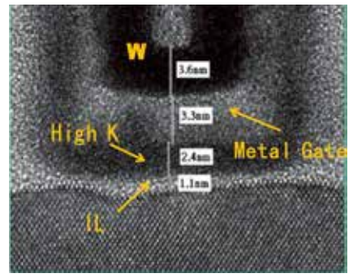


22 纳米全后栅 CMOS 集成技术

22nm All-Last HK/MG CMOS Integration Technique

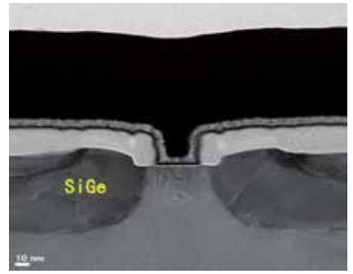
研究集体主要科技贡献：

研究集体主要科技贡献：该研究集体在国家科技重大专项支持下，牵头组织全国性产学研用联盟，联合北京大学、清华大学、复旦大学、中芯国际、武汉新芯等产学研用单位，通过 5 年攻关，实现了 22 纳米高 K 介质 / 金属栅工程、14 纳米 FinFet 器件、新型闪存器件、可制造性设计等关键技术的突破，研究水平迈入世界前列；提出了“专利指导下的研发战略”，在关键工艺模块上形成了较为系统的知识产权布局（专利 2406 项，含国际专利 483 项），并首次实现了向大型制造企业的许可转让，开始进入产业化开发阶段。这一成果的取得，标志着我国在集成电路这一高度全球化的高科技竞争领域前沿开始拥有一席之地，将为我国纳米级极大规模集成电路产业技术升级提供有力的技术支撑。



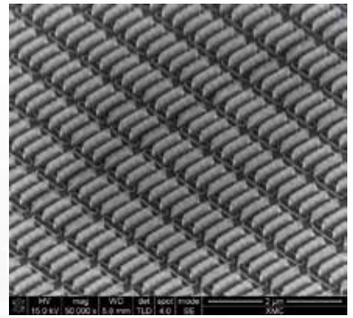
22 纳米高 K/ 金属栅工程

22nm High-k/Metal Gate Engineering



22 纳米源漏与沟道工程

22nm Source/Drain and Channel Engineering



大规模高密度 FinFET 阵列 （三维视图）

Large Scale & High Density FinFET Array (3D View)

研究集体突出贡献者

叶甜春 Ye Tianchun

叶甜春

主要科技贡献：负责技术路线整体设计与规划、知识产权系统布局和实施，组建“产学研”联合研发团队，推进技术研发与产业化。

陈大鹏 Chen Dapeng

陈大鹏

主要科技贡献：负责组织 22 和 14 纳米关键工艺技术研发，重点攻关任务推进，组建集成电路先导工艺公共研发平台。

朱慧珑 Zhu Huilong

朱慧珑

主要科技贡献：负责技术攻关，提出了“专利指导下的研发战略”，领导形成了 20-14 纳米主要专利组合，在高 K/ 金属栅和 FinFET 方面，截止到 2013 年个人专利申请数量全球排名分别为第一和第五。

研究集体主要完成者

赵 超　闫 江　杨士宁　徐秋霞　刘 明　陈 岚　殷华湘　钟汇才
尹海洲　李俊峰　王文武　霍宗亮　李春龙　王红丽　王大海　阮文彪
唐 波